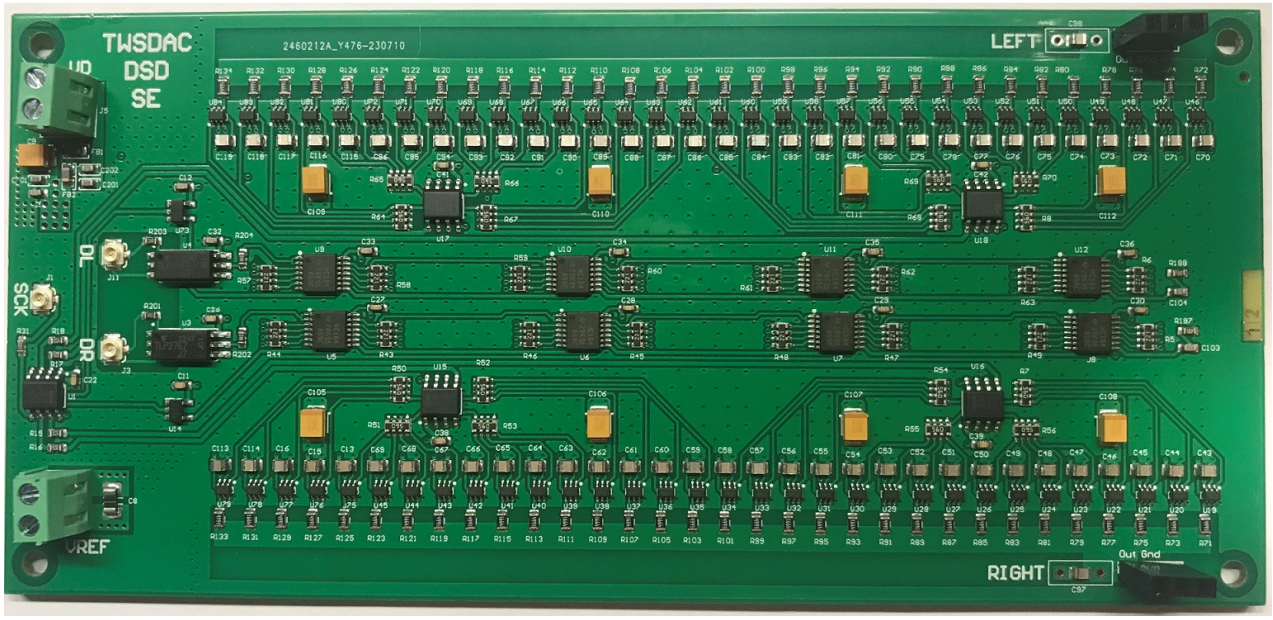
# TWSDAC-DSD-SE The Well Segmented DAC discrete DSD Single Ended




The TWSDAC-DSD-SE is a single ended DSD discrete DAC which accepts up to DSD512 sample rate.

The TWSAFB-LT FIFO buffer and the TWSAFB-XMOS USB receiver provide the DSD output to feed the DAC in single ended architecture and RTZ mode (Return to Zero). The DSD DAC can even work when driven by any other source which provides standard DSD output without RTZ.

RTZ mode is strongly recommended to get the best performance from the DSD DAC.

Moreover, when the TWSDAC-DSD is driven by the TWSAFB-LT FIFO buffer or the TWSAFB-XMOS USB receiver, the serial clock comes directly from the master clock. This allows the best jitter performance since the most critical signal does not cross any active device. Using the FIFO buffer or the USB receiver, the max allowed sample rate is dictated by the master clock: DSD128 (DSD64 in RTZ mode) with 5.6448 MHz and 6.144 MHz oscillators, DSD256 (DSD128 in RTZ mode) with 11.2896 MHz and 12.288 MHz oscillators and DSD512 (DSD26 in RTZ mode) with 22.5792 MHz and 24.576 MHz oscillators.

The dirty part of the incoming signals are optically isolated to avoid any interference with the crucial signal for the DAC, which is the SCK.

The DAC works in continuous clock mode.

The output impedance is around 160 ohm, it can easily drive the most preamplifiers and amplifiers.

Digital (VDD) and analog (Vref) power supplies are separated to get better isolation between the digital and the analog parts of the DAC.

22.5792 MHz and 24.576 MHz DRIXO oscillators (TWTMC-DRIXO) are recommended to get the best performance from the DSD DAC.

The DAC can operate with Return to Zero logic when driven by the TWSAFB-LT FIFO Lite or by the TWSAFB-XMOS receiver in order to null the rise/fall time errors which occurs in the bit switches.

In RTZ mode the master clock must be at least double of the DSD serial clock, for example with 22.5792 MHz and 24.576 MHz the DAC runs in RTZ logic up to DSD256, while the RTZ is not applied at DSD512.

Features:

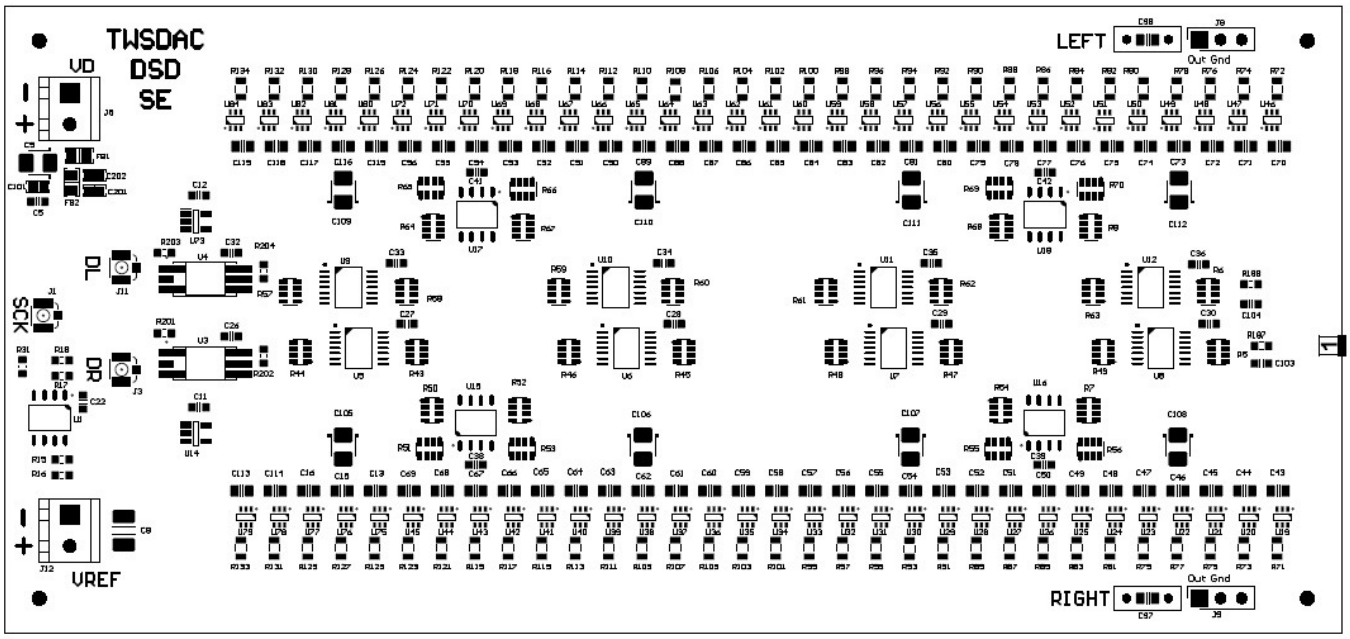
**Inputs:** standard DSD (provided by the TWSAFB-LT FIFO buffer, TWSAFB-XMOS or any other source)
**Format:** up to DSD512 (up to DSD256 in RTZ mode)
**Architecture:** single ended
**Clock mode:** continuous clock
**Master clock:** 5.6448/6.144 MHz up to DSD128 (DSD64 RTZ), 11.2896/12.288 MHz up to DSD256 (DSD128 RTZ), 22.5792/24.576 MHz up to DSD512 (DSD256 RTZ)
**RTZ logic:** Return to Zero logic available when driven by the TWSAFB-LT or TWSAFB-XMOS
**Isolation:** DATA signals optically isolated
**Output:** voltage output 0.7V rms (0.35V rms in RTZ mode) with Vref=4VDC
**Power supply:** digital VDD +3.3VDC to +5VDC 300 mA, analog Vref +3.3VDC to +5VDC 150 mA
**Board size:** 163 x 76 mm

**Note:** finished board (stereo).

The DAC operates in single ended architecture, so there is a DC offset at the analog output (+1V or +0.5V in RTZ mode).

The TWTSEBX4 single ended line buffer is recommended to null the offset and provide the suitable gain (up to 1.8V rms). The line buffer fits the DAC board.

## PCB layout




## Connectors

**J1:** SCK, serial clock input

**J3:** DR, right channel data input

**J11:** DL, left channel data input

**J8:** Left analog output (Out, Ground)

**J9:** Right analog output (Out, Ground)

**J5:** VDD Digital power supply, +3.3VDC to +5VDC 150 mA

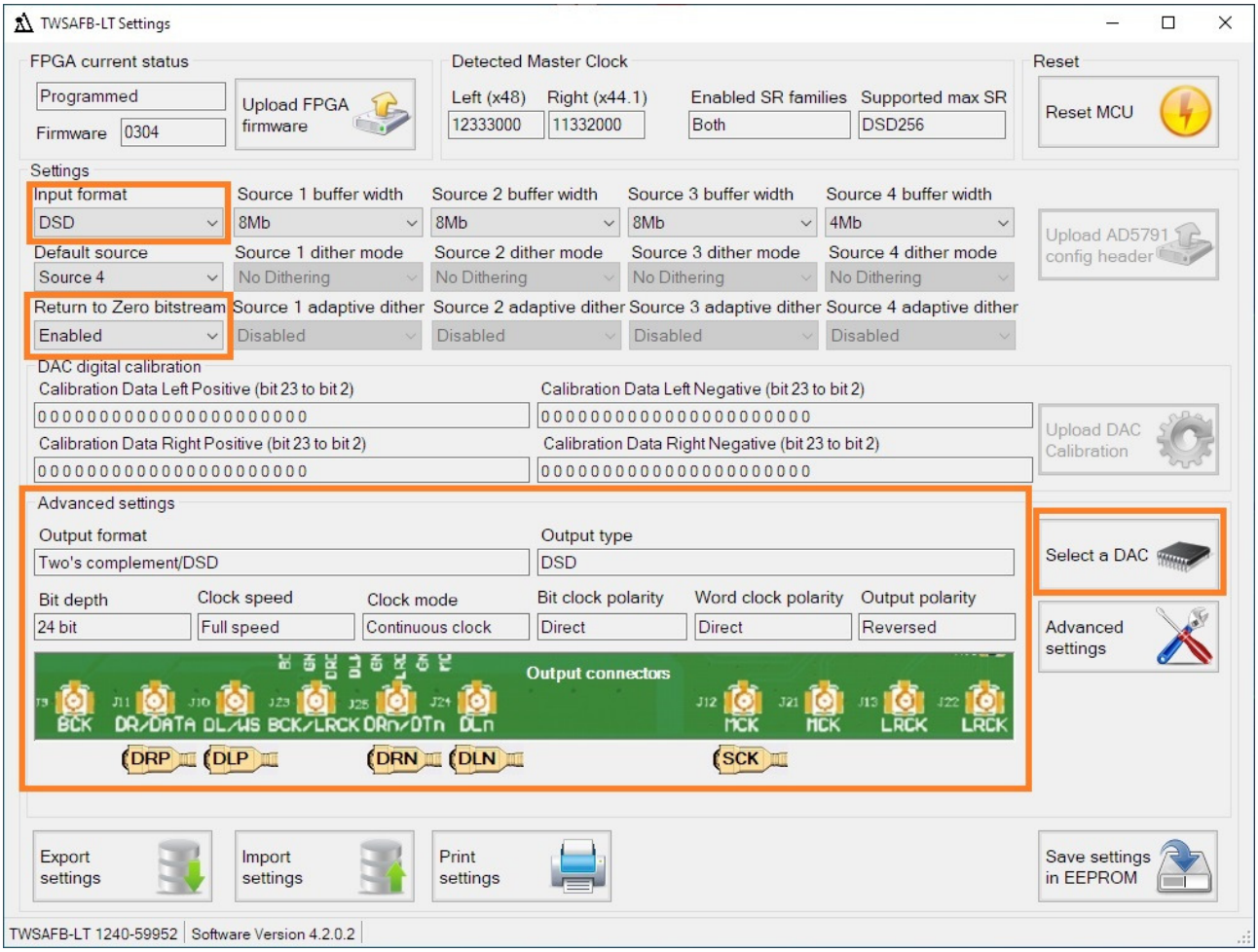
**J12:** Vref Analog power supply, +3.3VDC to +5VDC 300 mA

### Settings

No settings are needed.

## Configuring and connecting to the TWSAFB-LT (FIFO Lite)

In order to get the DAC working, the TWSAFB-LT has to be configured as below:




1. Download, install and open the TWSAFB-LT Settings Windows application
2. Connect the TWSAFB-LT to a PC by USB
3. Wait until the device is detected
4. Press "Select a DAC" and select the "TWSDAC-DSD discrete DAC DSD input" from the DAC database
5. Enable Return to Zero bitstream if you want the DAC working with RTZ logic (recommended)
6. Press "Save in EEPROM" to store the settings in the TWSAFB-LT memory
7. Disconnect the USB from the TWSAFB-LT
8. Connect the DAC board using short u.fl cables: FIFO DR/DATA to DAC DR, FIFO DL/WS to DAC DL, FIFO MCK to DAC SCK
9. Connect a I2S source to the selected "Default source"

**Configuring and connecting to the TWSAFB-XMOS (USB receiver)**

In order to get the DAC working, the TWSAFB-USB has to be configured as below

1. Set TWSAFB-XMOS Phase by on board dip-switches: BCK=On, DATA=Off, LRCK=Off
2. Enable DSD RTZ if you want the DAC working with RTZ logic (recommended) by on board dip-switch: DSD RTZ=On
3. Connect the DAC board using short u.fl cables: XMOS DATA/DL to DAC DL, XMOS LRCK/DR to DAC DR, XMOS MCK/SCK to DAC SCK
4. Connect a USB source to the TWSAFB-XMOS

**Warning**

The DAC does include a simple 6dB/octave low pass filter at its output, 2.2 nF capacitor (C97 and C98). You can replace these capacitors with others in the range 1 nF to 4.7 nF as on your taste.

VDD power supply has to be equal or greater than 0.75 x Vref. For example, if Vref is powered by 4.5VDC then VDD has to be powered by at least 3.4 VDC. In this case, even the clean side of the TWSAFB-LT (J18) has to be powered by the same 3.4 VDC.

Using the TWSAFB-XMOS as source, max allowed VDD is 4VDC since the clean side of the USB receiver is powered with 3V3DC.

**DAC output**

Since the DAC has DC offset you have 2 options to connect it to preamp/amp:

1. Using the TWTSEBX4 single ended line buffer which nulls the DC offset and provides suitable gain to drive preamp/amp (see User Manual)
2. Direct capacitor coupled if DAC output voltage is compliant with your preamp/amp