TWSAFB-USB The Well Synchronized Asynchronous FIFO buffer

USB receiver

The TWSAFB-USB is an asynchronous USB receiver intended to isolate the DAC from the source, getting them operating in different and fully isolated time domains. This way the jitter of the source cannot affect the DAC. Practically the incoming I2S/DSD data are processed by an XMOS processor which works in slave mode. This means that the outgoing data are synchronized in a different time domain managed by the master clock and optically isolated from the incoming data, preventing source jitter from crossing the receiver and affecting the DAC. In practice, this allows the output signals to be regenerated starting from a much more precise clock than that of the source.

The TWSAFB-USB receiver provides digital outputs to drive most of the DAC on the market, sigma-delta and I2S DACs. It provides I2S and DSD output.

The USB receiver has to be connected to an USB source like a PC running Windows, Linux or Mac OS.

The outputs are available on 8-pin JST headers compliant with the input connectors of the TWSAFB-LT FIFO buffer.

The part of the circuit containing the master clock is powered separately and isolated from the rest of the circuit which handles the input signals.

The TWSAFB-USB has two master clock on board (NDK NZ2520SDA oscillators at 45.1584 and 49.152 MHz).

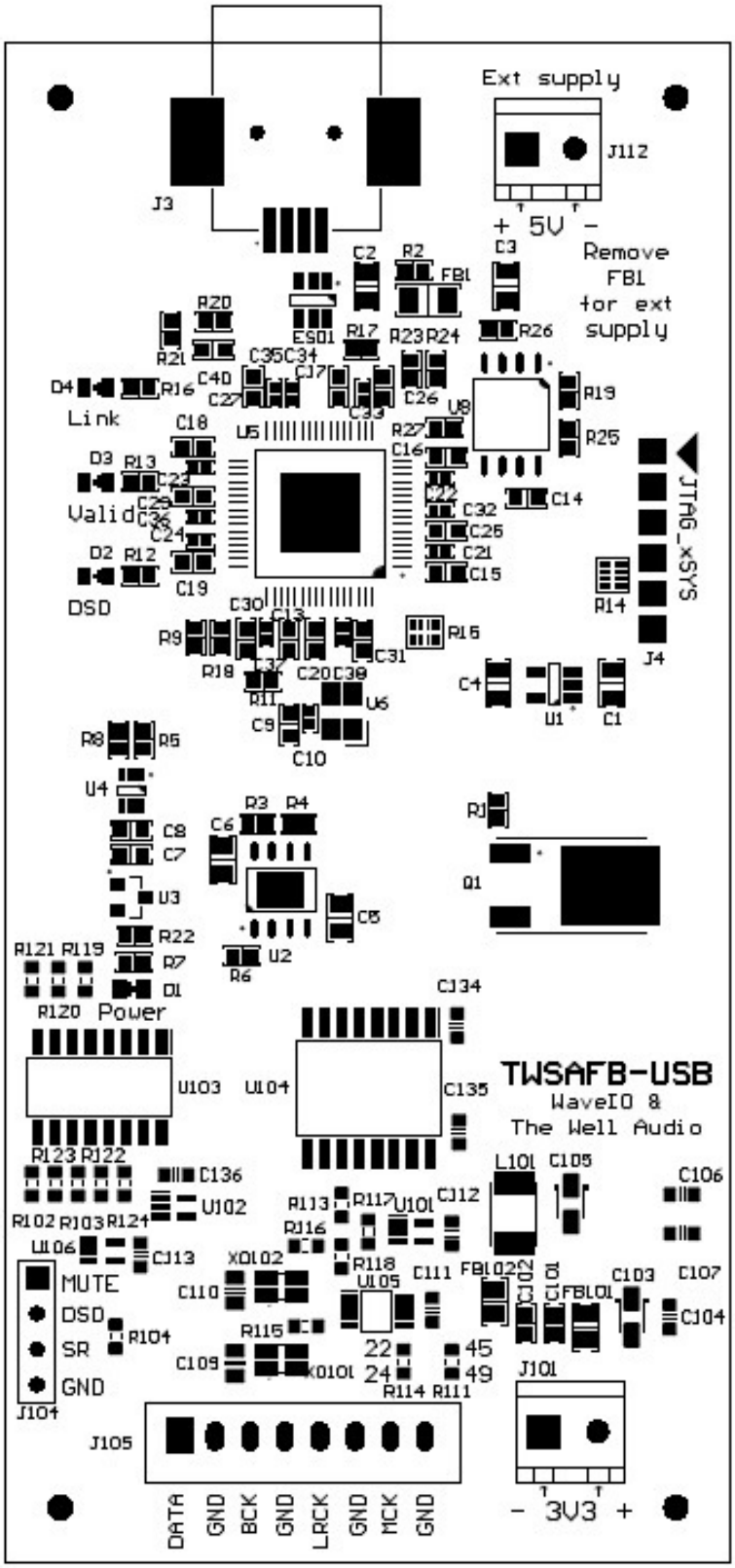
It provides selectable Master clock output at 45.1584/49.152 MHz or 22.5792/24.576 MHz.

Features:

Input format: I2S/DoP/DSD
Inputs: USB port
Output format: PCM up to 768 kHz, DSD up to DSD512
Galvanic isolation: all output signals are galvanic isolated from the XMOS processor to avoid interferences from the source
Master clock output: selectable (45.1584/49.152 MHz or 22.5792/24.576 MHz)
Power supply: 3V3DC/100 mA (isolated side)
External power supply: optional 5VDC/300 mA (USB side)
Software: ASIO driver for Windows provided
Board size: 109 x 52 mm

Note: finished board

PCB layout


Ext supply
J112
+ 5V -
Remove
FB1
for ext
supply
J3
C2
R2
FB1
C3
R26
R20
R21
ES01
R17
R23
R24
C35
C34
C40
C27
C17
C33
C26
D4
R16
Link
U8
R19
R25
C18
U5
R27
C16
D3
R13
Valid
C32
C14
C25
C21
C15
JTAG_xSYS
D2
R12
DSD
C19
C30
C13
R14
J4
R9
R16
C31
R18
C37
C20
C38
U6
C4
U1
C1
R11
C9
C10
R8
R5
U4
R3
R4
C6
C8
C7
U3
C5
R1
Q1
R22
R7
U2
R6
R121
R119
D1
R120
Power
C134
U103
U104
C135
TWSAFB-USB
WaveIO &
The Well Audio
R123
R122
C136
L101
C105
C106
R102
R103
R124
U102
R113
R117
U101
C112
R116
U106
C113
XO102
R118
C111
FB102
C102
C101
FB101
C103
C107
C110
U105
C104
MUTE
DSD
SR
GND
R104
R115
22
24
45
49
C109
XO101
R114
R111
J101
J104
J105
DATA
GND
BCK
GND
LRCK
GND
MCK
GND
- 3V3 +

Connectors

J3: USB input

J101: Isolated side power supply (mandatory), 3.3 VDC/50 mA

J112: Optional external USB power supply, 5 VDC/300 mA (remove FB1 if used)

J105: Isolated I2S/DSD output

1. DATA, I2S DATA or DSD Right Data
2. GND, Ground
3. BCK, I2S Bit clock or DSD SCK
4. GND, Ground
5. LRCK, I2S WS or DSD Left Data
6. GND, Ground
7. MCK, Master clock (45.1584/49.152 MHz or 22.5792/24.576 MHz)
8. GND, Ground

J104: Isolated Status outputs

1. MUTE, Mute signal (Low: the audio data stream is not valid and the DAC must be muted; High: the audio data stream is valid)
2. DSD, Audio Stream Format (Low: PCM; High: DSD)
3. SR, Sample rate family (Low: x44.1 kHz family; High: x48 kHz family)
4. GND, Ground

J4: Reserved

Master clock output options

R114: 22.5792/24.576 MHz (as provided)

R111: 45.1584/49.152 MHz (remove R114 and install on R111 footprint)

Led status indicators

D1: Power, USB side of the board is powered on

D2: DSD, Audio stream format is DSD

D3: Valid, Valid audio stream detected (mute status when off)

D4: Link, USB side of the board is connected to the source

External power supply option

In order to provide external power supply to the USB side of the board, the following steps has to be suited:

1. Remove FB1 from the board
2. Provide regulated 5VDC/300 mA to J112 (pay attention to the polarity of the header)